2M x 8 11/10 EDO DRAM

Features

- 2,097,152 word by 8 bit organization
- Single 3.3V ± 0.3V or 5.0V ± 0.5V power supply
- Standard Power (SP) and Low Power (LP)
- 2048 Refresh Cycles
  - 32 ms Refresh Rate (SP version)
  - 128 ms Refresh Rate (LP version)
- High Performance:

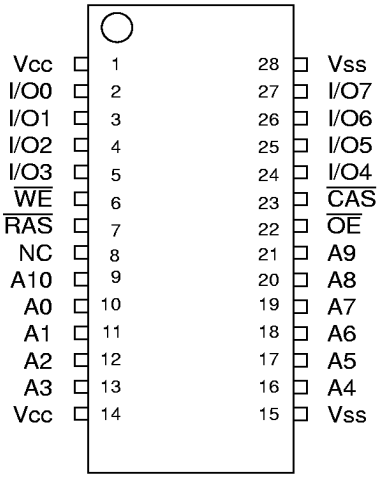
		-50	-60	-6R	-70	Units
t_{RAC}	$\overline{RAS}$ Access Time	50	60	60	70	ns
t_{CAC}	$\overline{CAS}$ Access Time	13	15	17	20	ns
t_{AA}	Column Address Access Time	25	30	30	35	ns
t_{RC}	Cycle Time	84	104	104	124	ns
t_{HPC}	EDO (Hyper Page) Mode Cycle Time	20	25	25	30	ns

- Low Power Dissipation
  - Active (max) - 100 mA / 90 mA / 80 mA
  - Standby: TTL Inputs (max) - 1.0 mA
  - Standby: CMOS Inputs (max)
    - 1.0 mA (SP version)
    - 0.2 mA (LP version)
  - Self Refresh (LP version only)
    - 200µA (3.3 Volt)
    - 300µA (5.0 Volt)
- Extended Data Out (Hyper Page) Mode
- Read-Modify-Write
- $\overline{RAS}$ Only and $\overline{CAS}$ before $\overline{RAS}$ Refresh
- Hidden Refresh
- Package: TSOP-II 28 (400milx725mil)

Description

The IBM0117805 is a dynamic RAM organized 2,097,152 words by 8 bits, which has a very low "sleep mode" power consumption option. These devices are fabricated in IBM's advanced 0.5µm CMOS silicon gate process technology. The circuit and process have been carefully designed to provide high performance, low power dissipation, and high reliability. The devices operate with a single 3.3V ± 0.3V or 5.0V ± 0.5V power supply. The 21 addresses required to access any bit of data are multiplexed (11 are strobed with $\overline{RAS}$, 10 are strobed with $\overline{CAS}$).

Pin Assignments (Top View)



Pin Description

$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
A0 - A10	Address Inputs
$\overline{OE}$	Output Enable
I/O0 - I/O7	Data Input/Output
V_{CC}	Power (+3.3V or +5.0V)
V_{SS}	Ground

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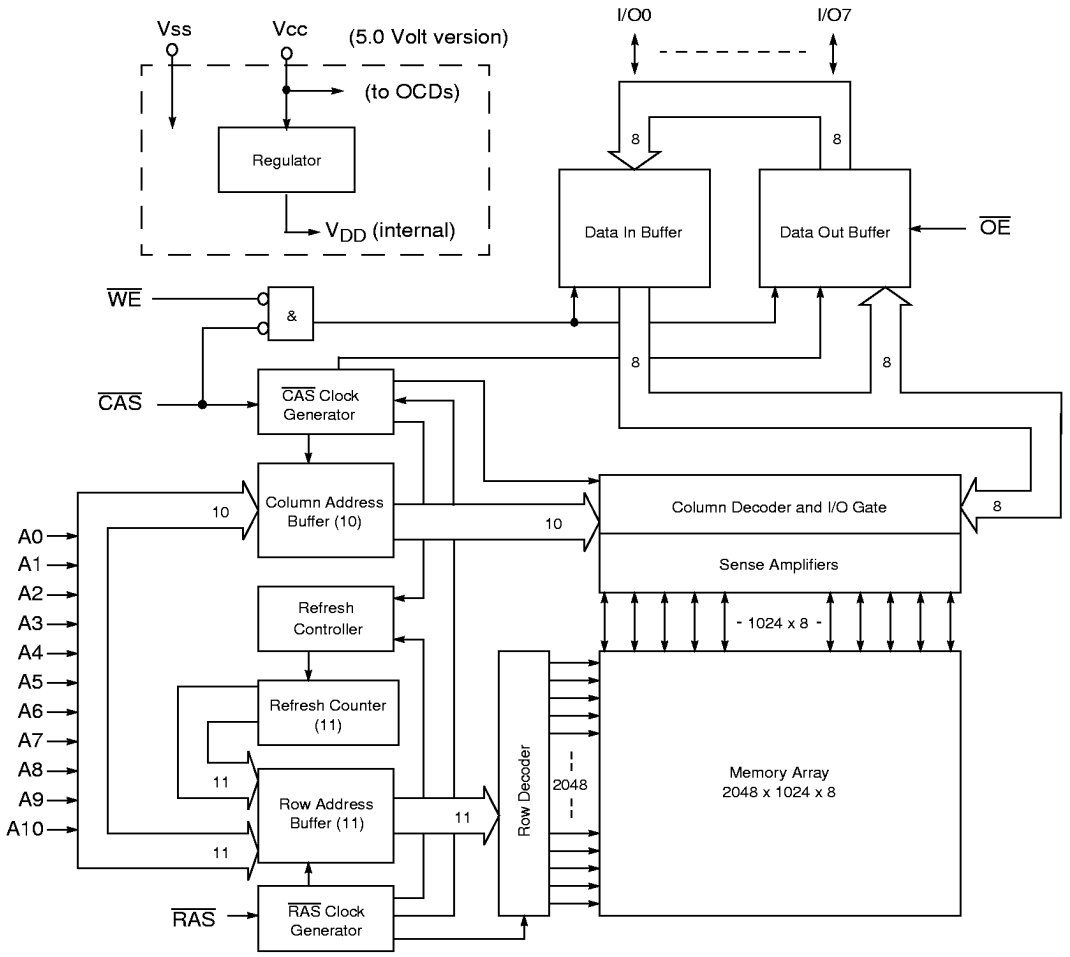
Ordering Information

Part Number	SP / LP	Self Refresh	Power Supply	Speed	Package	Notes
IBM0117805T3 -50	SP	No	5.0V	50ns	400mil TSOP-II 28	1
IBM0117805T3 -60	SP	No	5.0V	60ns	400mil TSOP-II 28	1
IBM0117805T3 -6R	SP	No	5.0V	60ns	400mil TSOP-II 28	1
IBM0117805T3 -70	SP	No	5.0V	70ns	400mil TSOP-II 28	1
IBM0117805BT3 -50	SP	No	3.3V	50ns	400mil TSOP-II 28	1
IBM0117805BT3 -60	SP	No	3.3V	60ns	400mil TSOP-II 28	1
IBM0117805BT3 -6R	SP	No	3.3V	60ns	400mil TSOP-II 28	1
IBM0117805BT3 -70	SP	No	3.3V	70ns	400mil TSOP-II 28	1
IBM0117805MT3 -50	LP	Yes	5.0V	50ns	400mil TSOP-II 28	1
IBM0117805MT3 -60	LP	Yes	5.0V	60ns	400mil TSOP-II 28	1
IBM0117805MT3 -70	LP	Yes	5.0V	70ns	400mil TSOP-II 28	1
IBM0117805PT3 -50	LP	Yes	3.3V	50ns	400mil TSOP-II 28	1
IBM0117805PT3 -60	LP	Yes	3.3V	60ns	400mil TSOP-II 28	1
IBM0117805PT3 -6R	LP	Yes	3.3V	60ns	400mil TSOP-II 28	1
IBM0117805PT3 -70	LP	Yes	3.3V	70ns	400mil TSOP-II 28	1

1. SP = Standard Power version (IBM0117805 and IBM0117805B); LP = Low Power version (IBM0117805M and IBM00117805P)

Block Diagram



Truth Table

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Col Address	I/O0 - I/O7
Standby		H	H→X	X	X	X	X	High Impedance
Read		L	L	H	L	Row	Col	Data Out
Early-Write		L	L	L	X	Row	Col	Data In
Delayed-Write		L	L	H→L	H	Row	Col	Data In
Read-Modify-Write		L	L	H→L	L→H	Row	Col	Data Out, Data In
EDO (Hyper Page) Mode Read	1st Cycle	L	H→L	H	L	Row	Col	Data Out
	2nd Cycle	L	H→L	H	L	N/A	Col	Data Out
EDO (Hyper Page) Mode Write	1st Cycle	L	H→L	L	X	Row	Col	Data In
	2nd Cycle	L	H→L	L	X	N/A	Col	Data In
EDO (Hyper Page) Mode Read-Modify-Write	1st Cycle	L	H→L	H→L	L→H	Row	Col	Data Out, Data In
	2nd Cycle	L	H→L	H→L	L→H	N/A	Col	Data Out, Data In
$\overline{RAS}$-Only Refresh		L	H	X	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh		H→L	L	H	X	X	N/A	High Impedance
Hidden Refresh	Read	L→H→L	L	H	L	Row	Col	Data Out
	Write	L→H→L	L	H	X	Row	Col	Data In
Self Refresh (LP version only)		H→L	L	L	H	X	X	X

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units	Notes
		3.3 Volt Device	5.0 Volt Device		
V_{CC}	Power Supply Voltage	-0.5 to +4.6	-1.0 to +7.0	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC}+0.5, 4.6)	-0.5 to min (V_{CC}+0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC}+0.5, 4.6)	-0.5 to min (V_{CC}+0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +150	-55 to +150	°C	1
P_D	Power Dissipation	1.0	1.0	W	1
I_{OUT}	Short Circuit Output Current	50	50	mA	1

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A= 0 to 70˚C)

Symbol	Parameter	3.3 Volt Device			5.0 Volt Device			Units	Notes
		Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{CC}	Supply Voltage	3.0	3.3	3.6	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.5	2.4	—	V_{CC} + 0.5	V	1, 2
V_{IL}	Input Low Voltage	-0.5	—	0.8	-0.5	—	0.8	V	1, 2

1. All voltages referenced to V_{SS}.
2. V_{IH} may overshoot to V_{CC} + 1.2V for pulse widths of ≤ 4.0ns with 3.3 Volt, or V_{CC} + 2.0V for pulse widths of ≤ 4.0ns (or V_{CC} + 1.0V for ≤ 8.0ns) with 5.0 Volt. Additionally, V_{IL} may undershoot to -2.0V for pulse widths ≤ 4.0ns with 3.3 Volt, or to -2.0V for pulse widths ≤ 4.0ns (or -1.0V for ≤ 8.0ns) with 5.0 Volt. Pulse widths measured at 50% points with amplitude measured peak to DC reference.

Capacitance (T_A= 25°C, V_{CC}= 3.3V ± 0.3V or V_{CC}= 5.0V ± 0.5V)

Symbol	Parameter	Min.	Max.	Units	Notes
C_{I1}	Input Capacitance (A0 - A10)	—	5	pF	1
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	—	7	pF	1
C_O	Output Capacitance (I/O0 - I/O7)	—	7	pF	1

1. Input capacitance measurements made with rise time shift method with $\overline{CAS}$ & $\overline{RAS}$ = V_{IH} to disable output.

DC Electrical Characteristics (T_A= 0 to +70˚C, V_{CC}= 3.3V ± 0.3V or V_{CC}= 5.0V ± 0.5V)

Symbol	Parameter		Min.	Max.	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min.)	-50	—	100	mA	1, 2, 3
		-60 / 6R	—	90		
		-70	—	80		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		—	1	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} min)	-50	—	100	mA	1, 3
		-60 / 6R	—	90		
		-70	—	80		
I_{CC4}	EDO (Hyper Page) Mode Current Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-50	—	60	mA	1, 2, 3
		-60 / 6R	—	50		
		-70	—	40		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)	SP version	—	1	mA	
		LP version	—	0.2		
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-50	—	100	mA	1, 3
		-60 / 6R	—	90		
		-70	—	80		
I_{CC7}	Self Refresh Current, LP version only Average Power Supply Current during Self Refresh CBR cycle with $\overline{RAS}$ ≥ t_{RASS} (min); $\overline{CAS}$ held low; $\overline{WE}$ = V_{CC} - 0.2V; Addresses and D_{IN} = V_{CC} - 0.2V or 0.2V.	3.3V	—	200	µA	
		5.0V	—	300		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} + 0.3V)), All Other Pins Not Under Test = 0V		-5	+5	µA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-5	+5	µA	
V_{OH}	Output Level (TTL) Output “H” Level Voltage (I_{OUT} = -2.0mA for 3.3V, or I_{OUT} = -5mA for 5.0V)		2.4	V_{CC}	V	
V_{OL}	Output Level (TTL) Output “L” Level Voltage (I_{OUT} = +2.0mA for 3.3V, or I_{OUT} = +4.2mA for 5.0V)		0.0	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ =V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ =V_{IH}.

AC Characteristics (T_A= 0 to +70°C, V_{CC}= 3.3V ± 0.3V or V_{CC}= 5.0V ± 0.5V)

1. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
2. AC measurements assume t_T=2ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Valid column addresses are A0 through A9.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-50		-60		-6R		-70		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Random Read or Write Cycle Time	84	—	104	—	104	—	124	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	30	—	40	—	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	8	—	10	—	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	50	10K	60	10K	60	10K	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	8	10K	10	10K	10	10K	12	10K	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	8	_	10	—	10	—	10	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	14	37	14	45	14	43	14	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	12	25	12	30	12	30	12	35	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	8	—	10	—	10	—	12	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	38	—	45	—	45	—	50	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	5	—	5	—	ns	
t_{OED}	$\overline{OE}$ to D_{IN} Delay Time	13	—	15	—	15	—	15	—	ns	3
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	0	—	0	—	0	—	0	—	ns	4
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	0	—	0	—	ns	4
t_T	Transition Time (Rise and Fall)	2	50	2	50	2	50	2	50	ns	5

1. Operation within the t_{RCD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
3. Either t_{CDD} or t_{OED} must be satisfied.
4. Either t_{DZC} or t_{DZO} must be satisfied.
5. AC measurements assume t_T=2ns.

Write Cycle

Symbol	Parameter	-50		-60 / -6R		-70		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{WCS}	Write Command Set Up Time	0	—	0	—	0	—	ns	1
t_{WCH}	Write Command Hold Time	7	—	10	—	12	—	ns	
t_{WP}	Write Command Pulse Width	7	—	10	—	12	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	7	—	10	—	12	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	7	—	10	—	12	—	ns	
t_{DS}	D_{IN} Setup Time	0	—	0	—	0	—	ns	2
t_{DH}	D_{IN} Hold Time	7	—	10	—	12	—	ns	2

1. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions are satisfied, the condition of the data out (at access time) is indeterminate.
2. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in Read-Modify-Write cycles.

Read Cycle

Symbol	Parameter	-50		-60		-6R		-70		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RAC}	Access Time from $\overline{RAS}$	—	50	—	60	—	60	—	70	ns	1, 2, 3
t_{CAC}	Access Time from $\overline{CAS}$	—	13	—	15	—	17	—	20	ns	1, 3
t_{AA}	Access Time from Address	—	25	—	30	—	30	—	35	ns	2, 3
t_{OEA}	Access Time from $\overline{OE}$	—	13	—	15	—	17	—	20	ns	3
t_{RCS}	Read Command Setup Time	0	—	0	—	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	0	—	0	—	ns	4
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	0	—	0	—	ns	4
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	25	—	30	—	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	0	—	0	—	ns	3
t_{OFF}	Output Buffer Turn-Off Delay	—	13	—	15	—	15	—	15	ns	5, 6
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	13	—	15	—	15	—	15	—	ns	7
t_{OEZ}	Output Buffer Turn-Off Delay from $\overline{OE}$	—	13	—	15	—	15	—	15	ns	5
t_{OES}	$\overline{OE}$ Setup Time Prior to $\overline{CAS}$	5	—	5	—	5	—	5	—	ns	
t_{ORD}	$\overline{OE}$ Setup Time Prior to $\overline{RAS}$ (Hidden Refresh)	0	—	0	—	0	—	0	—	ns	

1. Operation within the t_{RCD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
3. Measured with the specified current load and 100pF at V_{OL} = 0.8V and V_{OH} = 2.0V.
4. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
5. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
6. t_{OFF} is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, which ever is last.
7. Either t_{CDD} or t_{OED} must be satisfied.

Read-Modify-Write Cycle

Symbol	Parameter	-50		-60		-6R		-70		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RWC}	Read-Modify-Write Cycle Time	115	—	135	—	135	—	162	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	67	—	79	—	79	—	94	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	30	—	34	—	36	—	44	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	42	—	49	—	49	—	59	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	7	—	10	—	10	—	12	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions are satisfied, the condition of the data out (at access time) is indeterminate.

Extended Data Out (Hyper Page) Mode Cycle

Symbol	Parameter	-50		-60 / -6R		-70		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{HCAS}	EDO (Hyper Page) Mode $\overline{CAS}$ Pulse Width	8	10K	10	10K	12	10K	ns	
t_{HPC}	EDO (Hyper Page) Mode Cycle Time (Read/Write)	20	—	25	—	30	—	ns	
t_{HPRWC}	EDO (Hyper Page) Mode Read Modify Write Cycle Time	51	—	60	—	72	—	ns	
t_{DOH}	Data-out Hold Time from $\overline{CAS}$	5	—	5	—	5	—	ns	
t_{WHZ}	Output buffer Turn-Off Delay from $\overline{WE}$	0	10	0	10	0	15	ns	
t_{WPZ}	$\overline{WE}$ Pulse Width to Output Disable at $\overline{CAS}$ High	7	—	10	—	10	—	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	30	—	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	28	—	35	—	40	ns	1
t_{RASP}	EDO (Hyper Page) Mode $\overline{RAS}$ Pulse Width	50	200K	60	200K	70	200K	ns	
t_{OEP}	$\overline{OE}$ Precharge	5	—	5	—	5	—	ns	
t_{OEHC}	$\overline{OE}$ High Hold Time from $\overline{CAS}$ High	5	—	5	—	5	—	ns	

1. Measured with the specified current load and 100pF at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.

Refresh Cycle

Symbol	Parameter	-50		-60 / -6R		-70		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	5	—	5	—	5	—	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	—	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	5	—	5	—	5	—	ns	

Self Refresh Cycle - Low Power version only

Symbol	Parameter	-50		-60		-70		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RASS}	$\overline{RAS}$ Pulse Width During Self Refresh Cycle	100	—	100	—	100	—	µs	1
t_{RPS}	$\overline{RAS}$ Precharge Time During Self Refresh Cycle	89	—	104	—	124	—	ns	1
t_{CHS}	$\overline{CAS}$ Hold Time From RAS Rising During Self Refresh Cycle	-50	—	-50	—	-50	—	ns	1, 2
t_{CHD}	$\overline{CAS}$ Hold Time From RAS Falling During Self Refresh Cycle	350	—	350	—	350	—	µs	1, 2

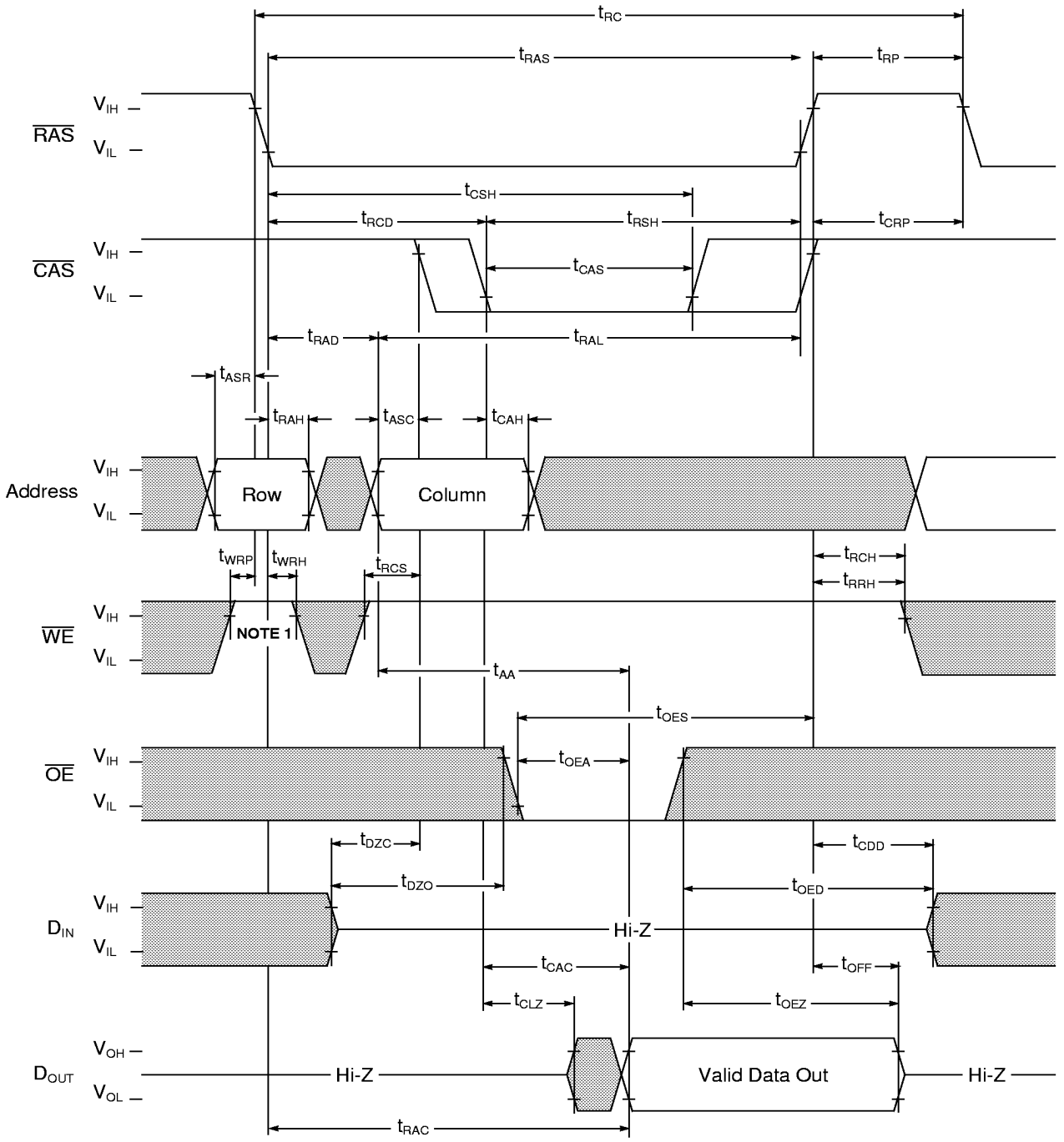
1. When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:
   If row addresses are being refreshed in an EVENLY DISTRIBUTED manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.
   If row addresses are being refreshed in any other manner (ROR- Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.
2. If $t_{RASS} > t_{CHD}$ (min) then t_{CHD} applies. If $t_{RASS} \leq t_{CHD}$ (min) then t_{CHS} applies.

Refresh

SYMBOL	Parameter		-50		-60 / -6R		-70		Units	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
t_{REF}	Refresh Period	SP version	—	32	—	32	—	32	ms	1
		LP version	—	128	—	128	—	128		

1. 2048 cycles.

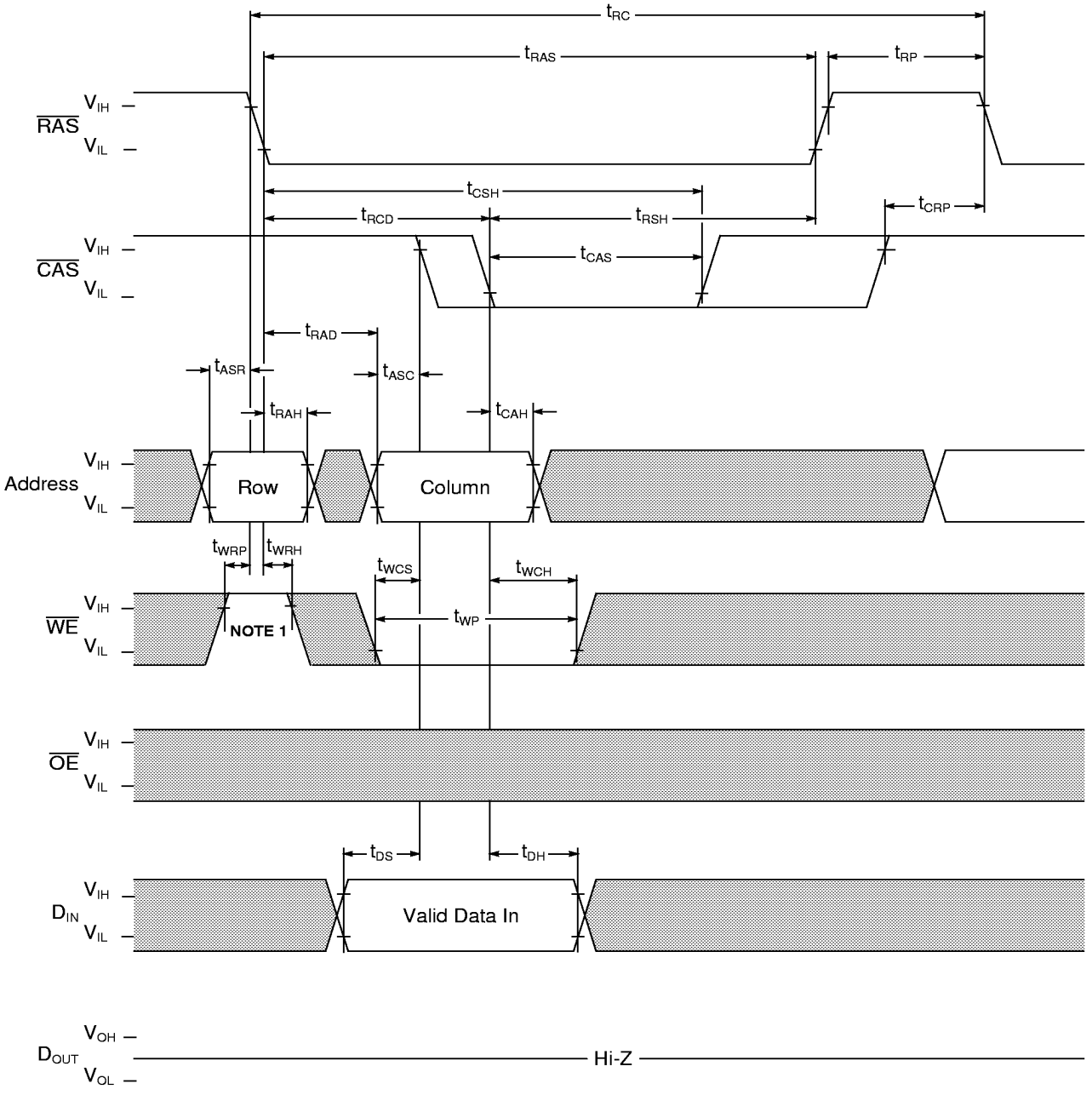
Read Cycle



: "H": or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

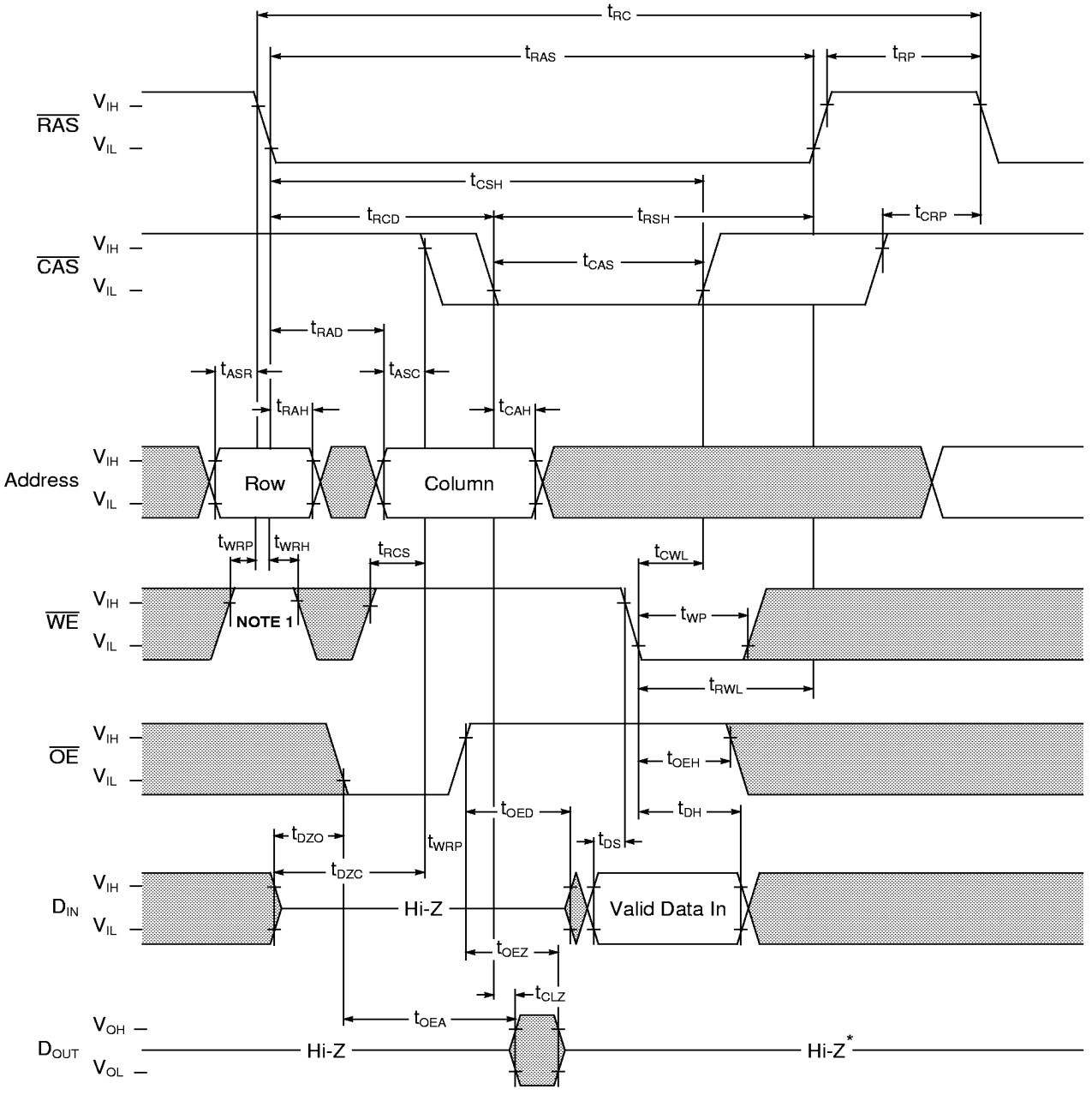
Write Cycle (Early Write)



: "H" or "L"

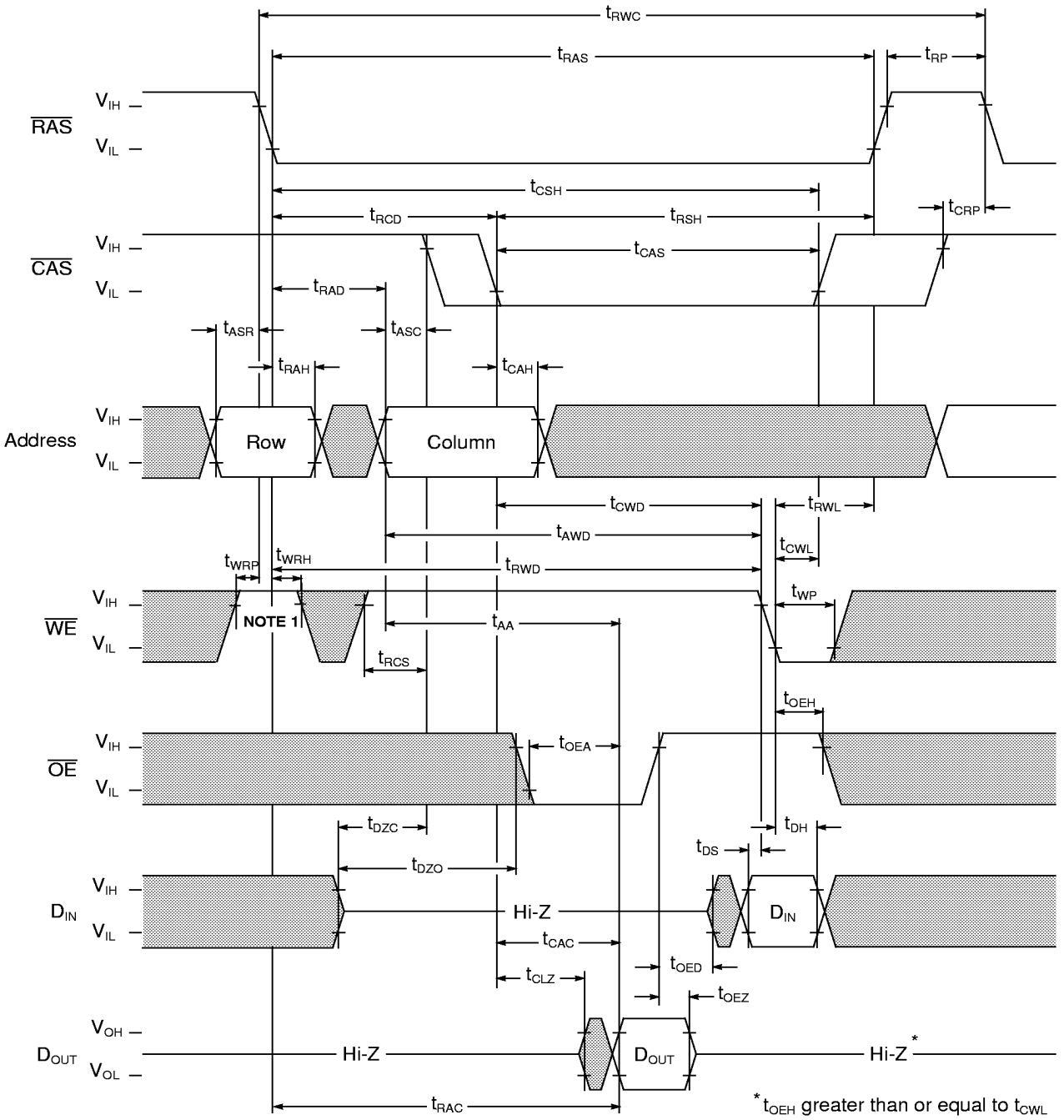
NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

Write Cycle (Delayed Write)



NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

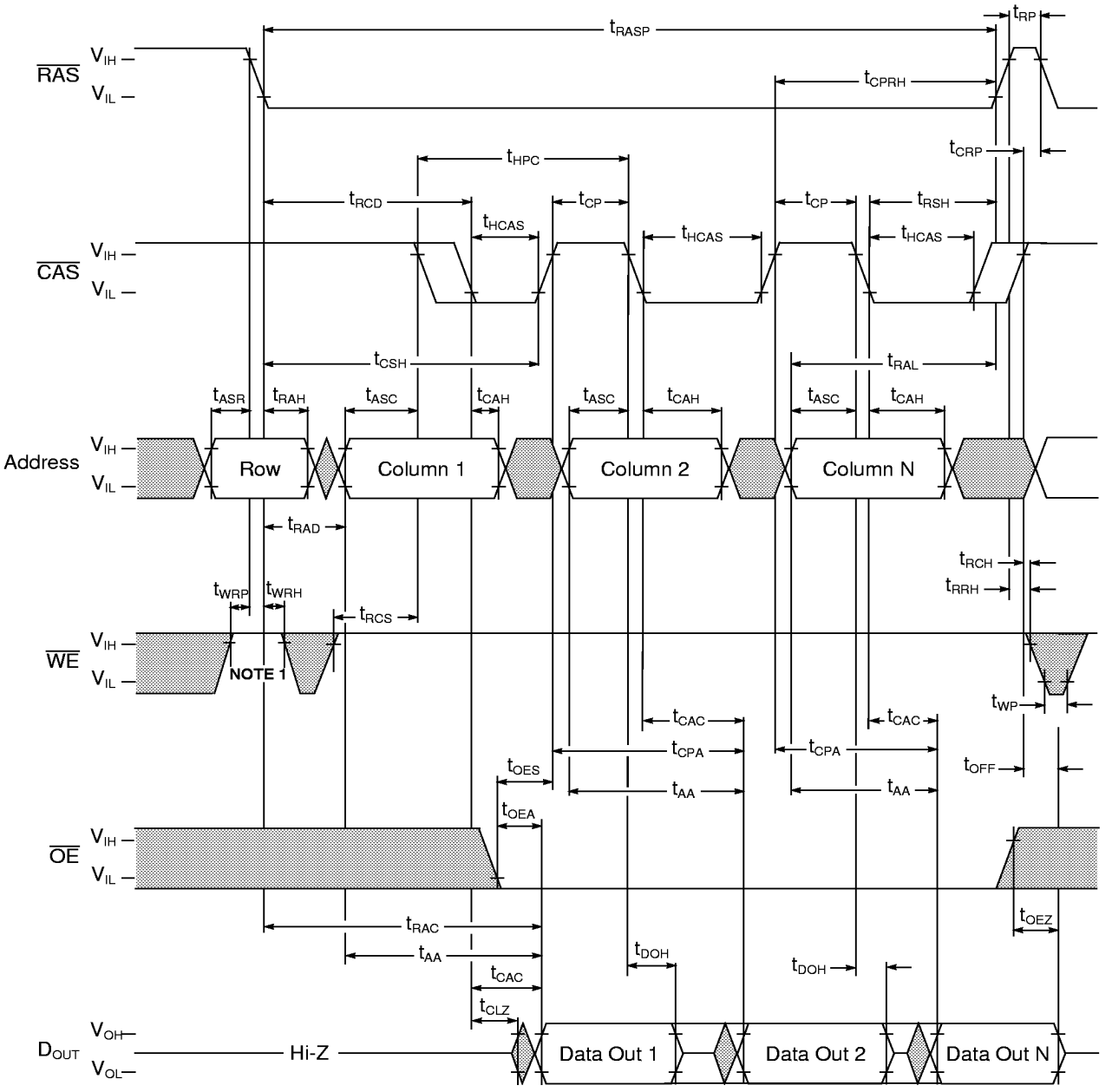
Read-Modify-Write Cycle



: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

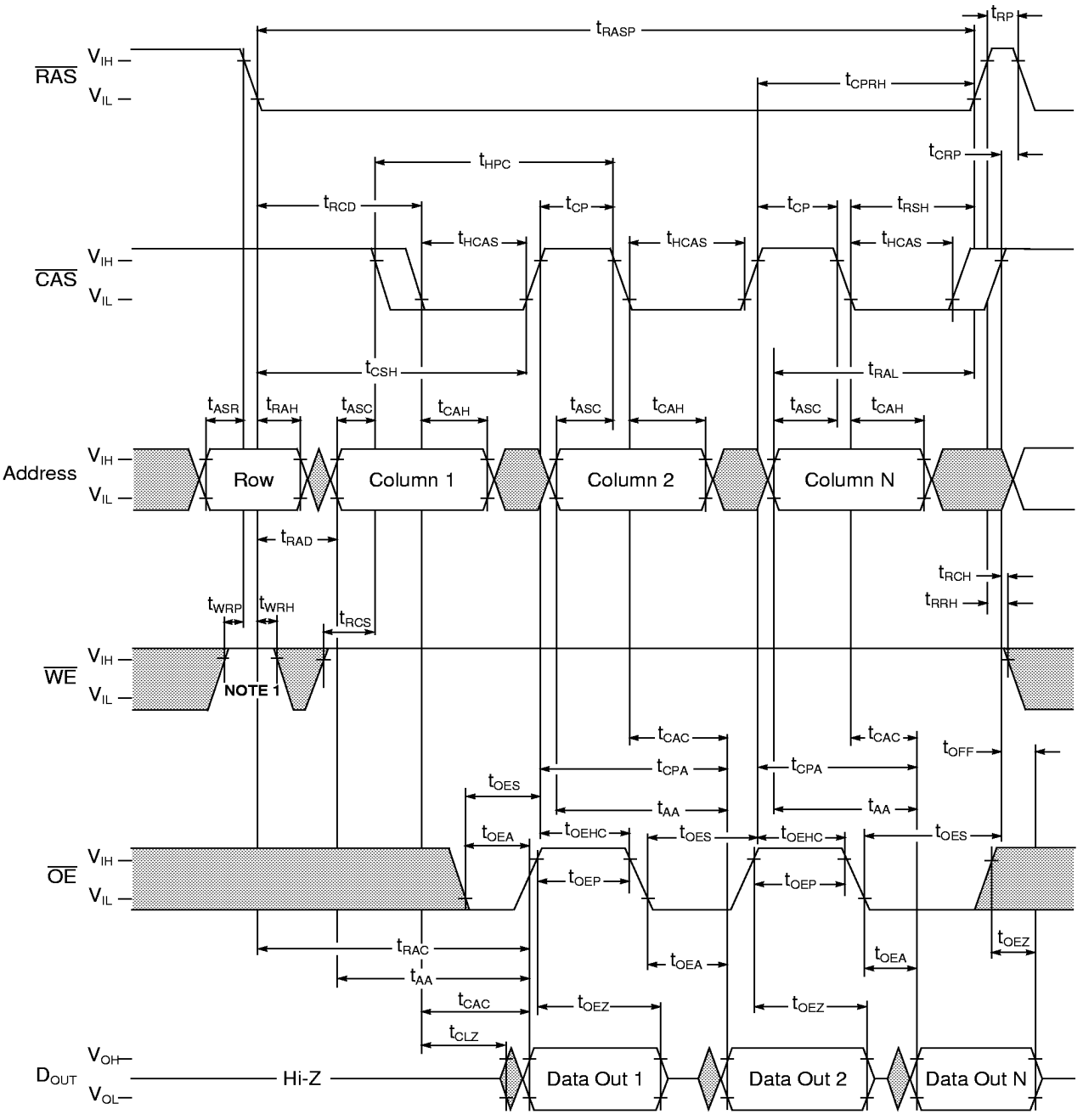
EDO (Hyper Page) Mode Read Cycle



: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

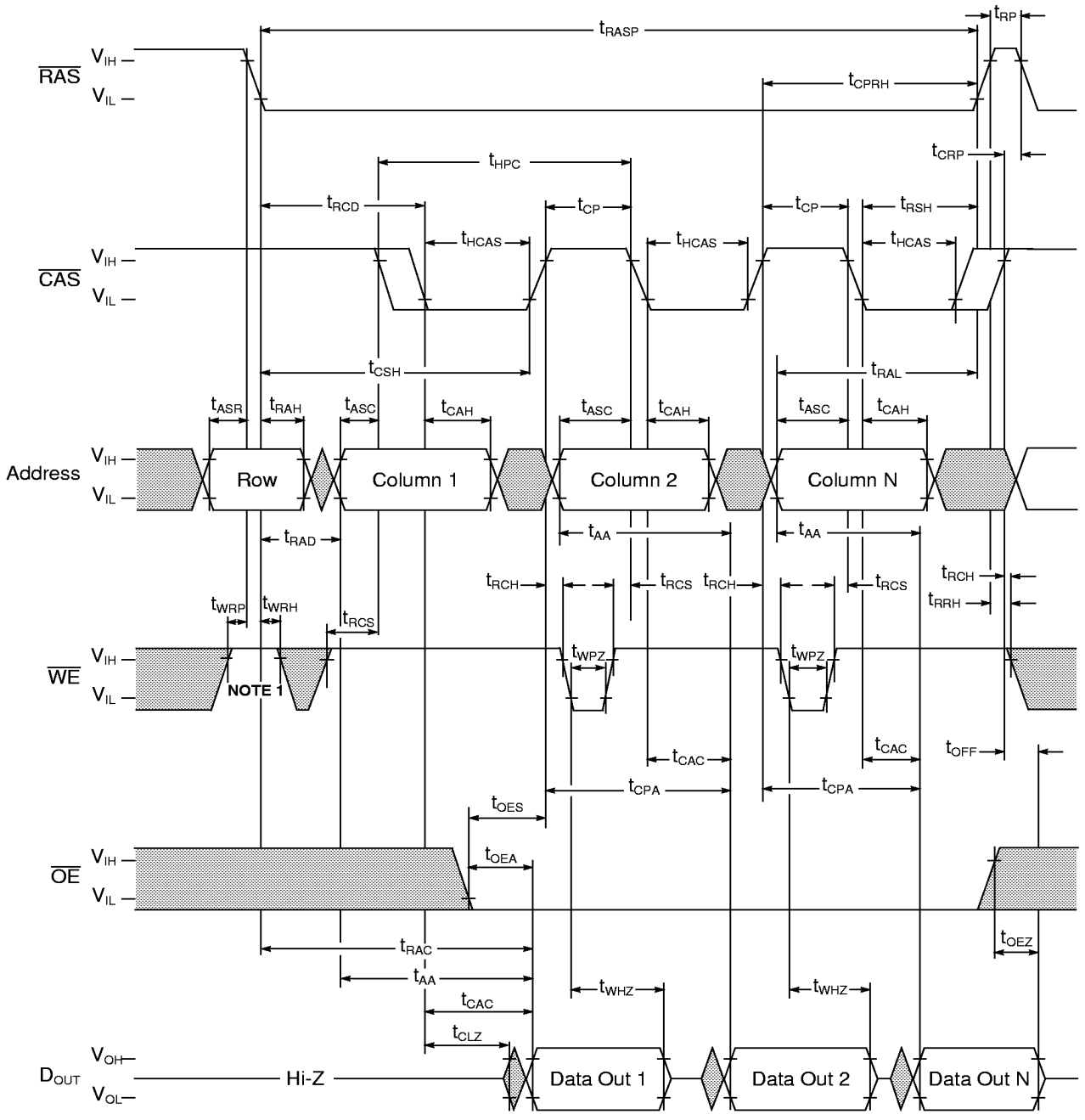
EDO (Hyper Page) Mode Read Cycle ($\overline{OE}$ Control)



: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

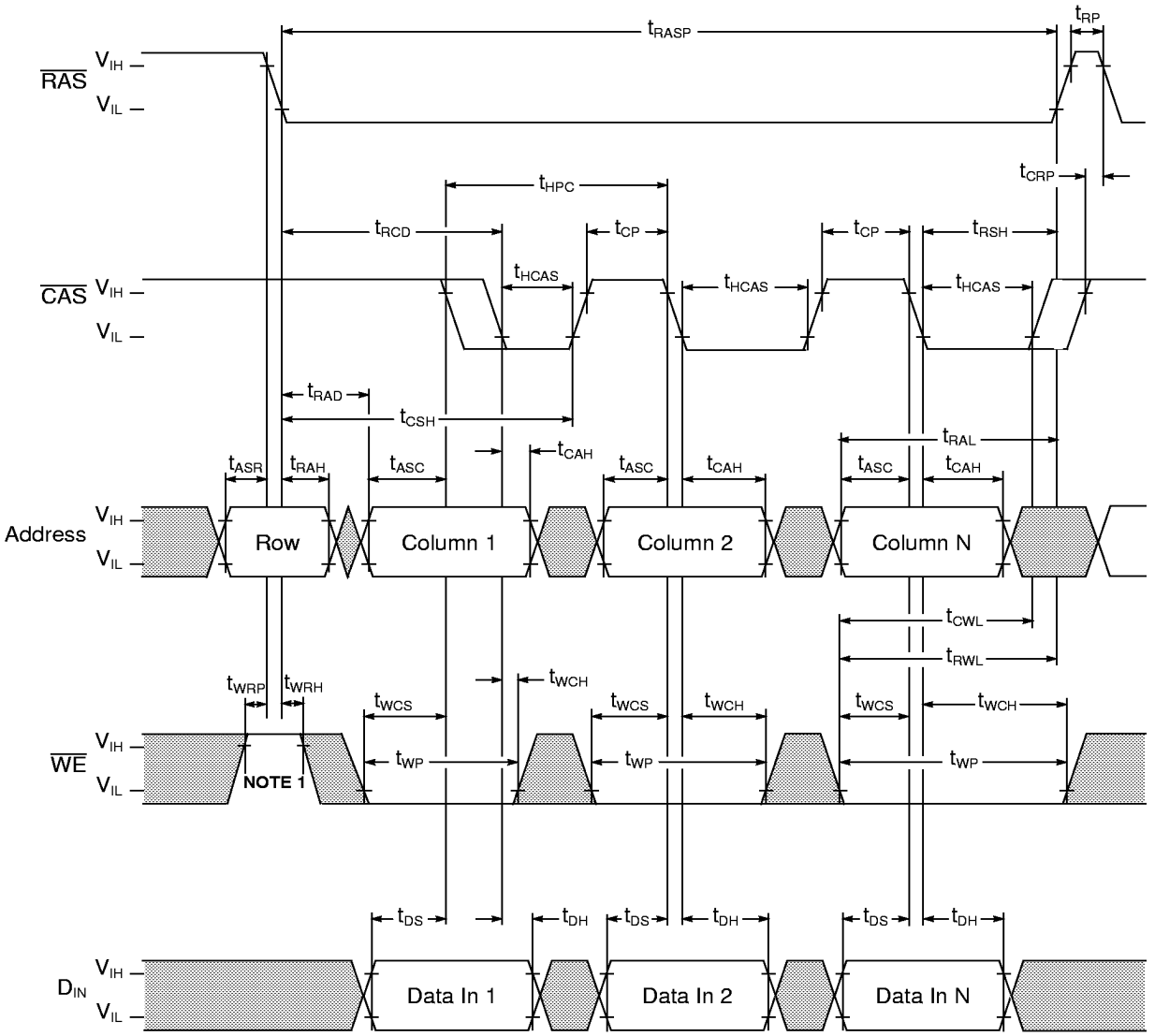
EDO (Hyper Page) Mode Read Cycle ($\overline{WE}$ Control)



: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

EDO (Hyper Page) Mode Early Write Cycle

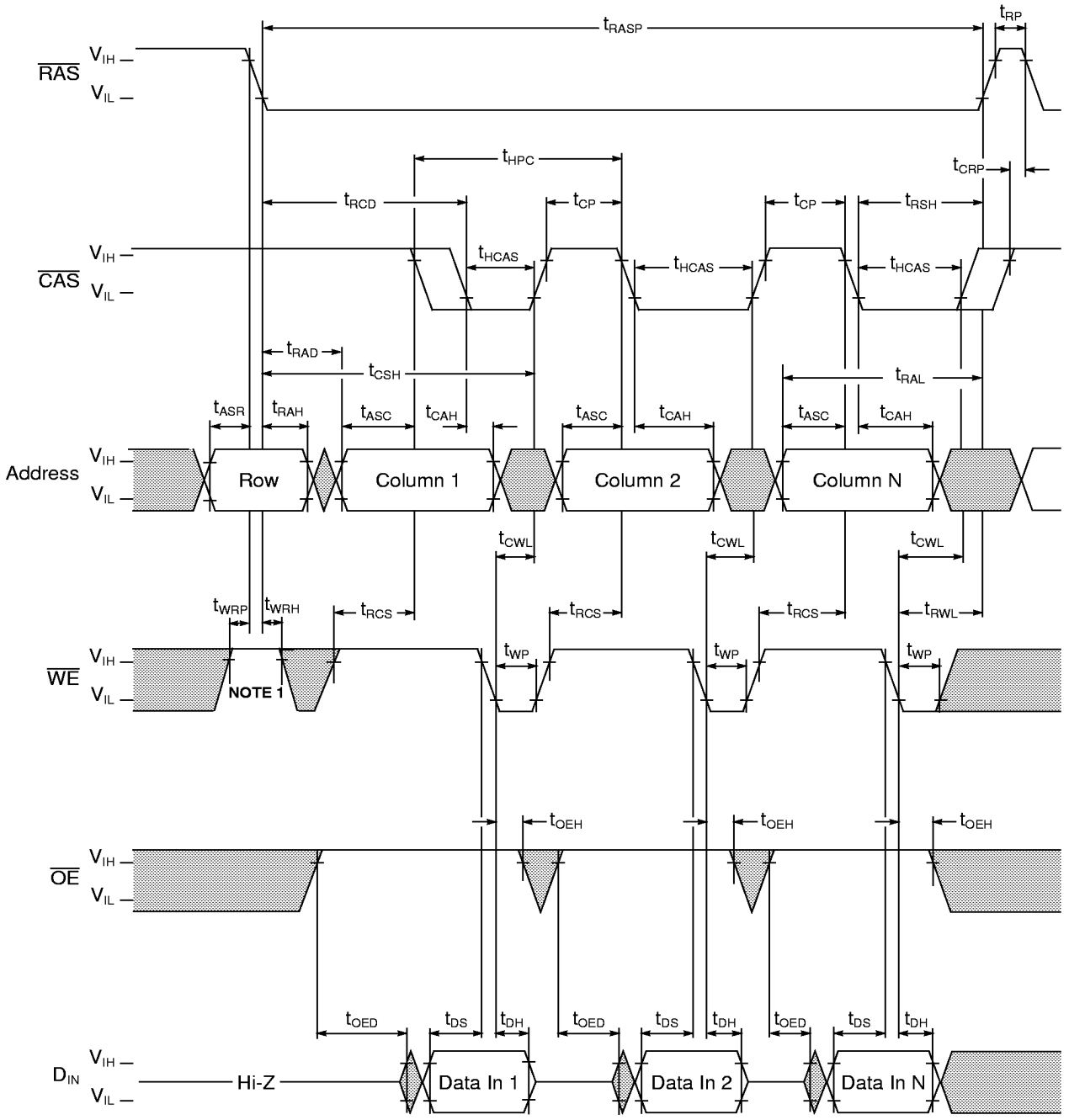


: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

$\overline{OE}$ = Don't care

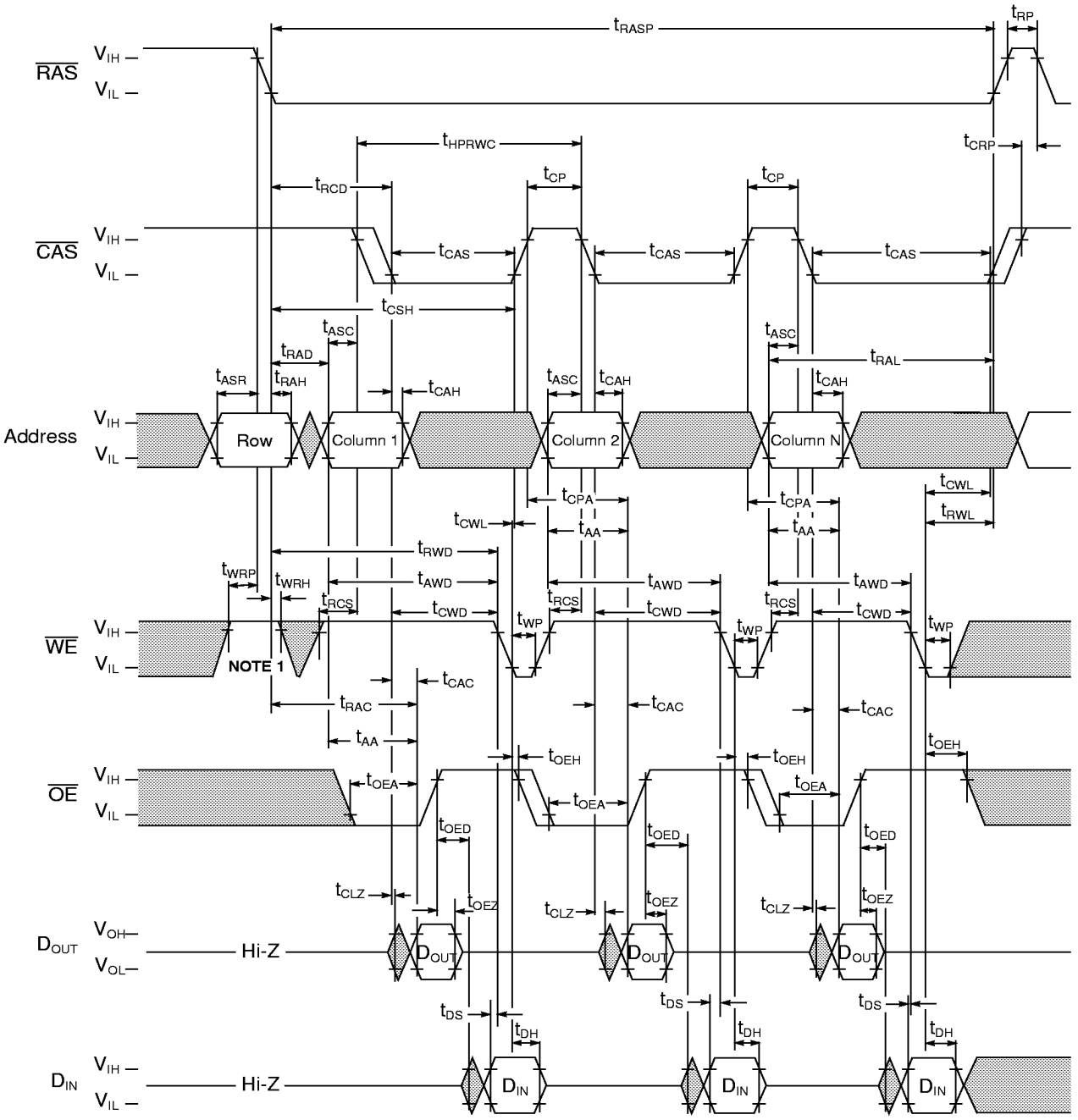
EDO (Hyper Page) Mode Late Write Cycle



: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

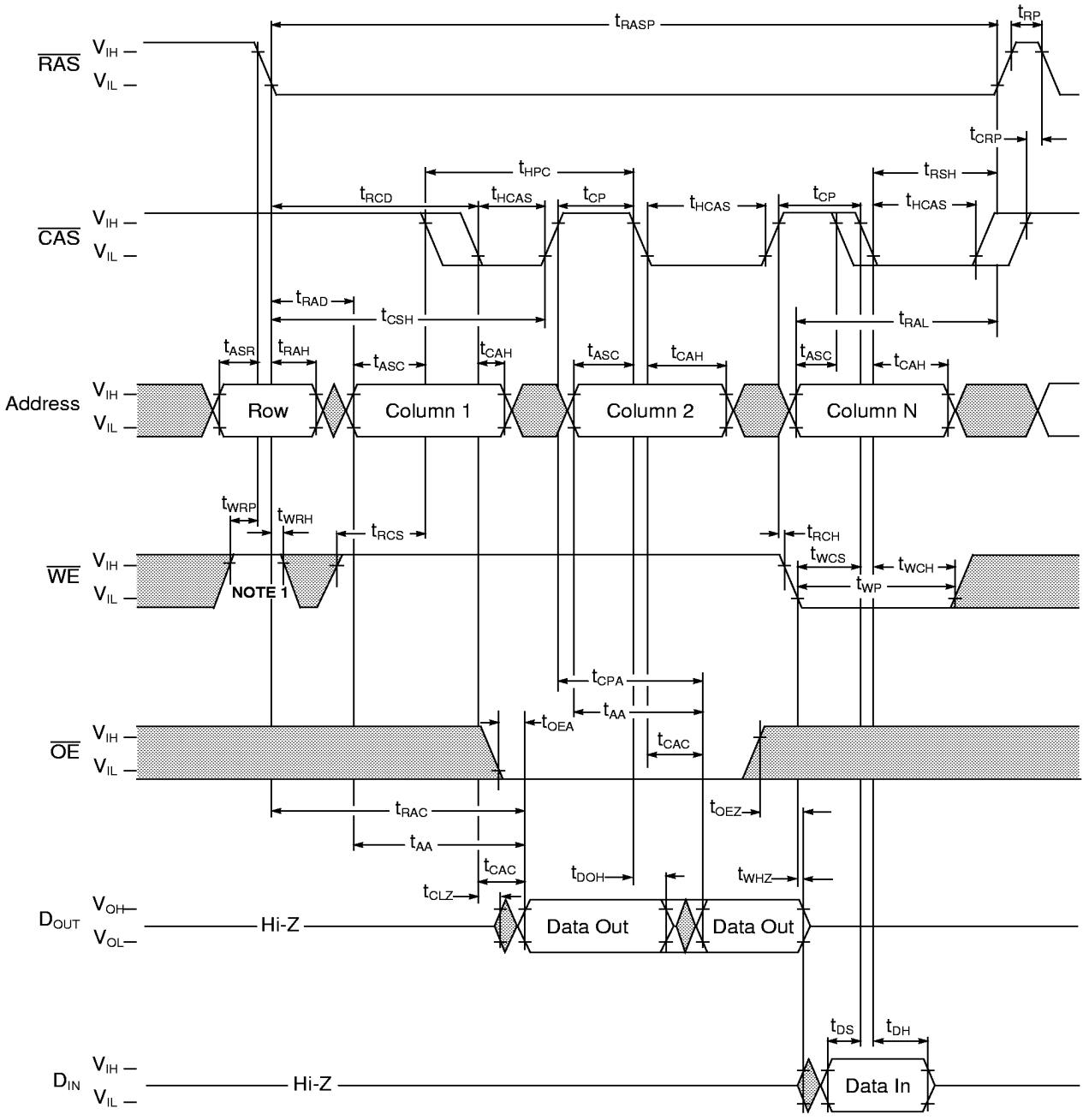
EDO (Hyper Page) Mode Read Modify Write Cycle



: "H" or "L"

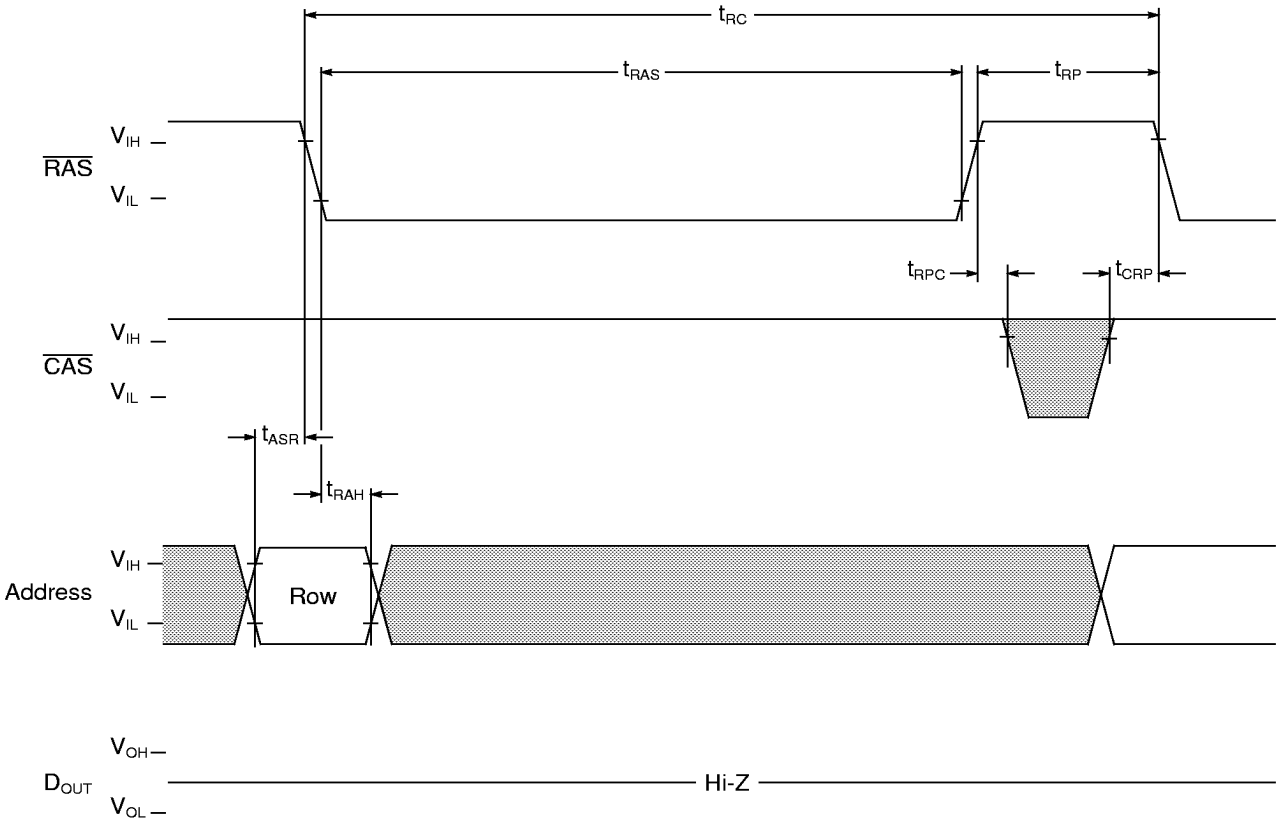
NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

EDO (Hyper Page) Mode Read and Write Cycle



NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

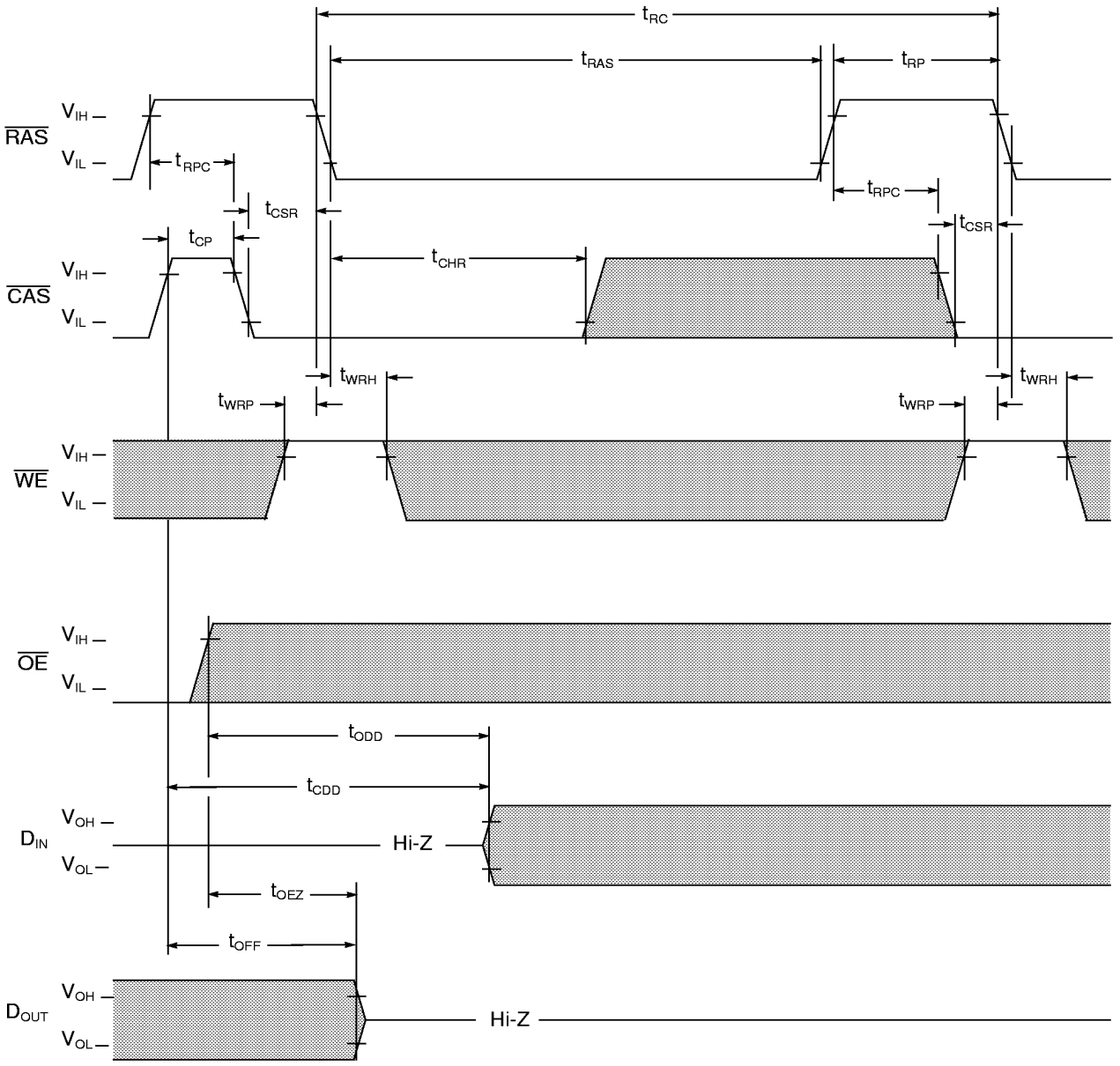
$\overline{RAS}$ Only Refresh Cycle



: "H" or "L"

NOTE : $\overline{WE}$, $\overline{OE}$ and D_{IN} are "H" or "L"

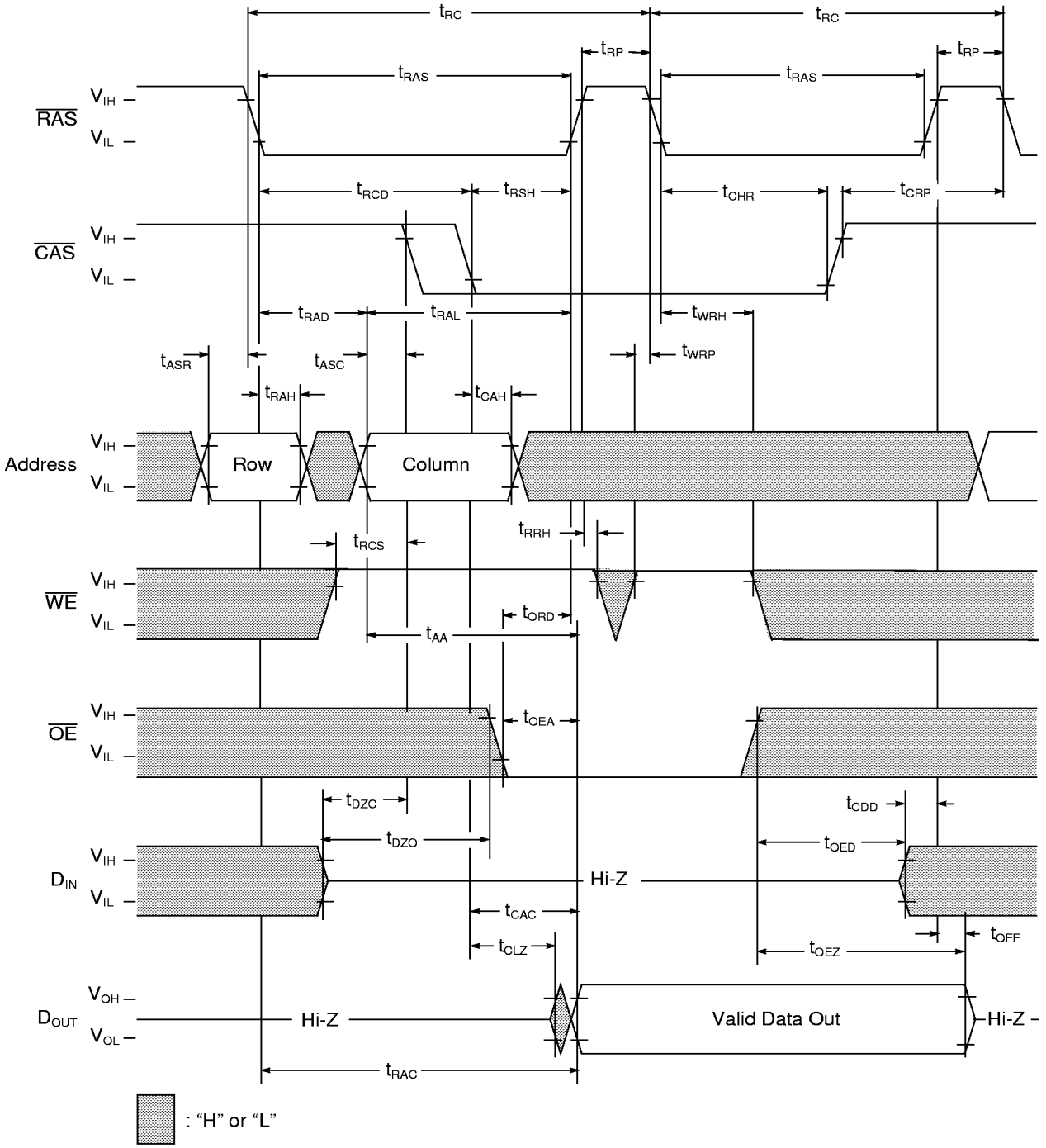
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



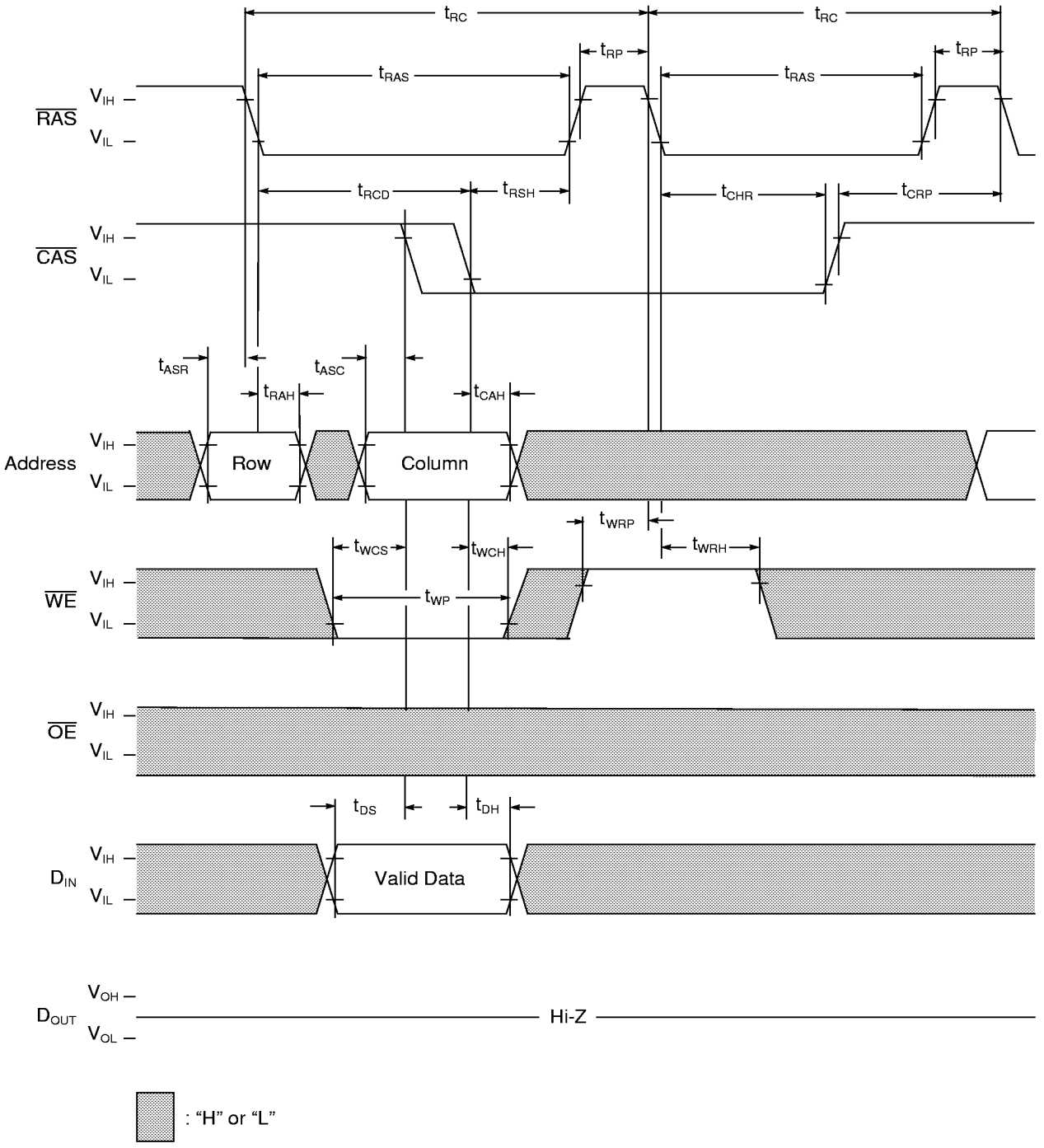
: "H" or "L"

NOTE: Address is "H" or "L"

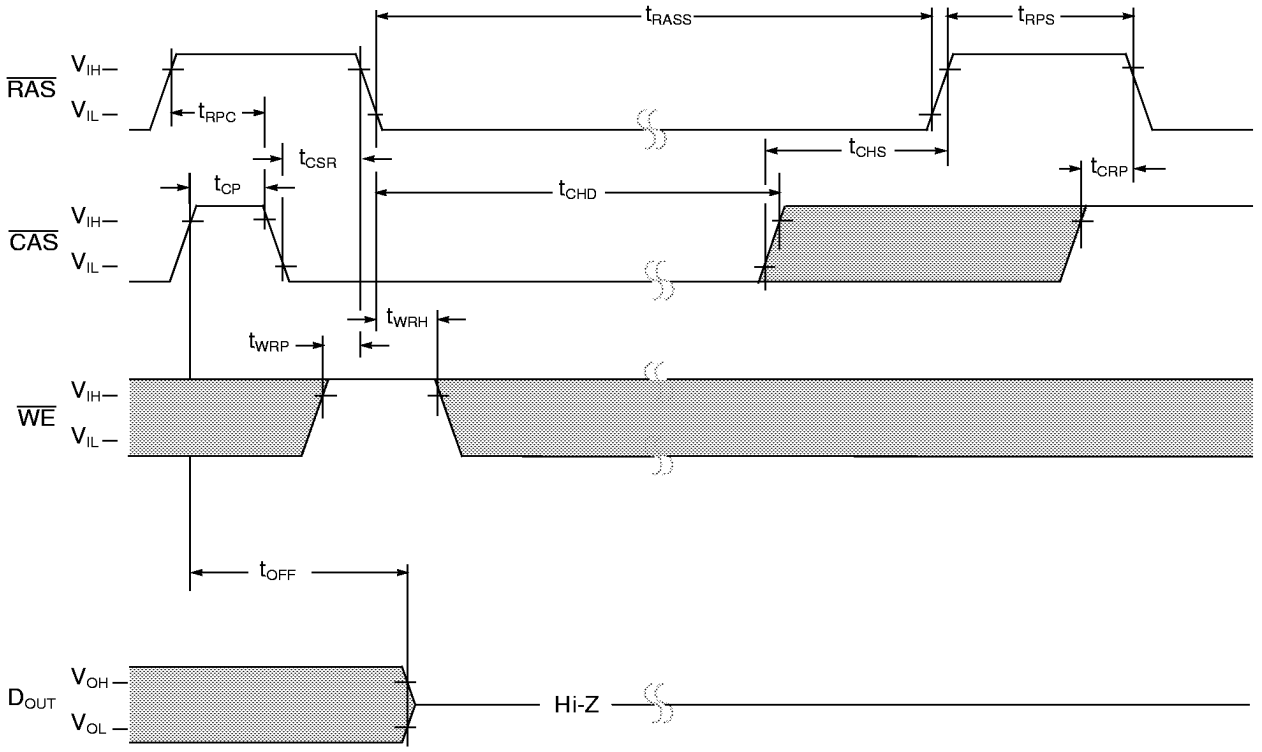
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)



Self Refresh Cycle (Sleep Mode) - Low Power version only

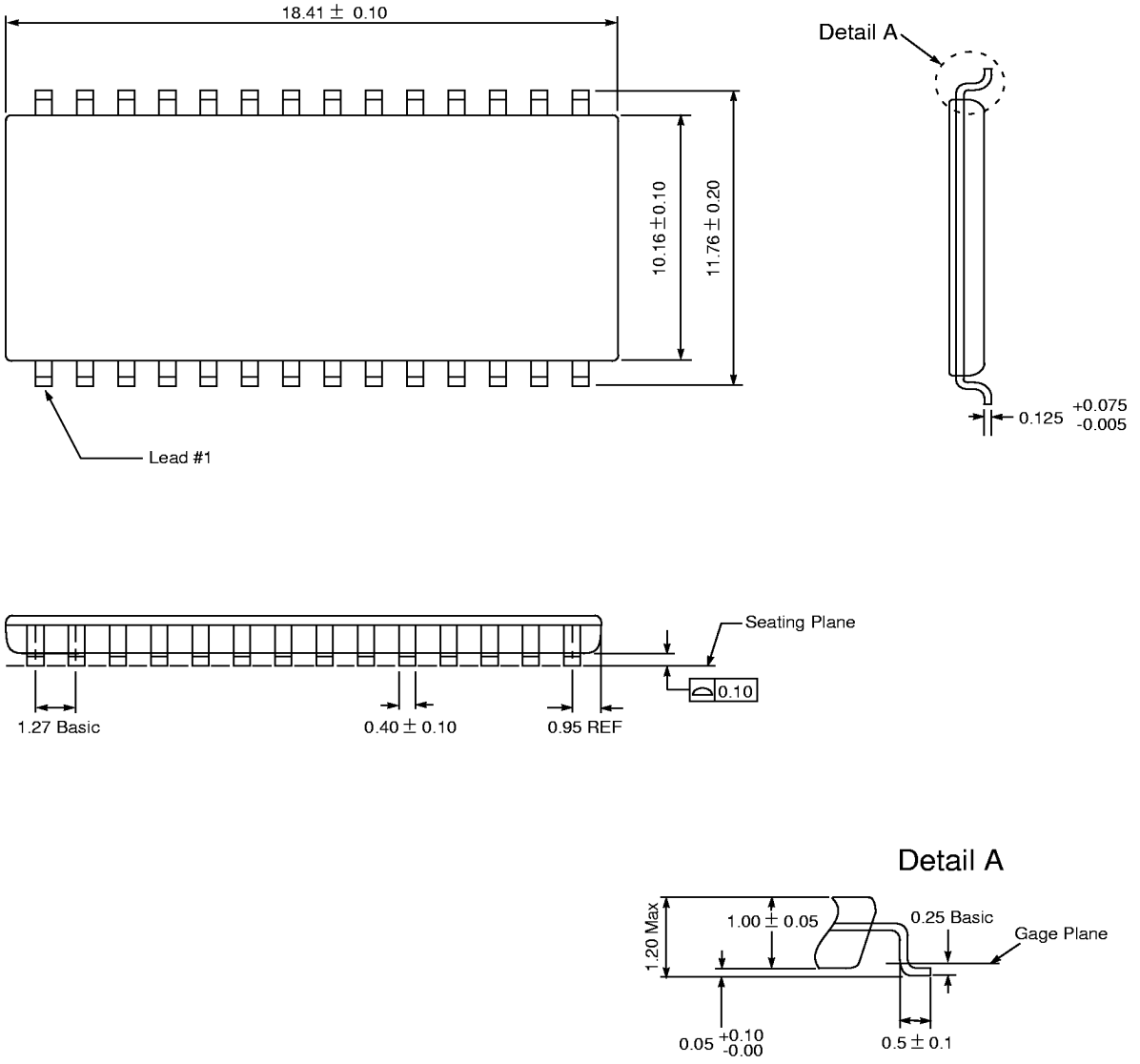


: "H" or "L"

NOTES:

1. Address and $\overline{OE}$ are "H" or "L"
2. Once $\overline{RAS}$ (min) is provided and $\overline{RAS}$ remains low, the DRAM will be in Self Refresh, commonly known as "Sleep Mode."
3. If $t_{RASS} > t_{CHD}$ (min) then t_{CHD} applies.
   If $t_{RASS} \leq t_{CHD}$ (min) then t_{CHS} applies.

Package Dimensions (400 mil; 28/28 lead; Thin Small Outline Package)



NOTE: All dimensions are in millimeters; Package diagrams are not drawn to scale

Revision Log

Revision	Contents Of Modification
11/15/95	Initial Release
12/10/95	1. The Low Power and Standard Power Specifications were combined. ES# 43G9060 and ES# 28H4724 were combined into ES# 28H4724. 2. Added Die Rev E part numbers. 3. A -6R speed sort was added, with the following differences over the -60 speed sort: - t_{CAC} was increased from 15ns to 17ns for the -6R speed sort - t_{RCD} (max) was decreased from 45ns to 43ns for the -6R speed sort. - t_{CWD} was increased from 34ns to 36ns for the -6R speed sort. - t_{OEA} was increased from 15ns to 17ns for the -6R speed sort. 4. t_{CHD} was added to the Self Refresh Cycle with a value of 350µs for all speed sorts. 5. The Self Refresh timing diagram was changed to allow $\overline{CAS}$ to go high t_{CHD} (350µs) after $\overline{RAS}$ falls entering a Self Refresh. 6. The CBR timing diagram was changed to allow $\overline{CAS}$ to remain low for back-to-back CBR cycles. 7. $\overline{WE}$ for the Hidden Refresh Write cycle in the Truth Table was changed from “L” to ” H”.
09/01/96	1. I_{CC2} was changed from 2mA to 1mA. 2. $I_{I(L)}$ and $I_{O(L)}$ were altered from +/- 10uA to +/- 5uA. 3. t_{RC} was changed from 89ns to 84ns for the -50 speed sort. 4. t_{CSH} changed from 45ns to 38ns, 50ns to 45ns, and 55ns to 50ns for the -50, -60, and -70 speed sorts, respectively. 5. t_T was initially at a max of 30ns. It has been modified to 50ns for all speed sorts. 6. t_{CPA} was decreased from 30ns to 28ns for the -50 speed sort. 7. t_{RASP} max of 125K was raised to 200K for all speed sorts. 8. t_{OEP} was changed from 10ns to 5ns for all speed sorts. 9. t_{OEHC} was also lowered from 10ns to 5ns for all speed sorts. 10. t_{RP} was changed from 35ns to 30ns for the -50 speed sort.